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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,716	07/31/2003	Shun-ichi Fukuyama	030860	9374
38834	7590	08/26/2004	EXAMINER	
WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP 1250 CONNECTICUT AVENUE, NW SUITE 700 WASHINGTON, DC 20036			SMOOT, STEPHEN W	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/630,716	Applicant(s) <sup>CA</sup> FUKUYAMA ET AL.	
	Examiner Stephen W. Smoot	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 31 July 2003.  
 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
 6) ☒ Claim(s) 1-10 is/are rejected.  
 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
 10) ☒ The drawing(s) filed on 31 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) ☒ All b) ☐ Some \* c) ☐ None of:  
 1. ☒ Certified copies of the priority documents have been received.  
 2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
 \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

This Office action is in response to application papers filed on 31 July 2003.

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Havemann (US 5,565,384).

Referring to Fig. 7, the Table bridging columns 6-7, and column 5, line 32 to column 6, line 45, Havemann (US 5,565,384) discloses an interconnect structure with the following features:

- A transistor structure formed on a substrate (40) with silicide (48) formed over source/drain regions and the gate electrode;
- A thin barrier layer (50) of TEOS (i.e. a first insulating film) formed over the transistor structure;

- An organic-containing low dielectric constant layer (54) (i.e. a second insulating film) formed over the barrier layer (50) (also see column 1, lines 56-64 and column 2, lines 34-36);
- Patterned conductors (18) that can be metal formed over the organic-containing layer (54) with conductive vias formed through the organic-containing layer (54) and the barrier layer (50) to electrically connect to the silicide (48) corresponding to the source/drain regions and the gate electrode of the transistor; and
- Additional levels of patterned conductors formed above the lower-most level (18) shown in Fig. 7 (also see column 6, lines 37-42).

These are all of the limitations set forth in claims 1-4 of the applicant's invention.

Regarding the method claims 8-9: the barrier layer (50) is a protective film; the use of TEOS implies deposition of the barrier layer (50) by chemical vapor deposition (CVD) because TEOS is a source gas used for depositing silicon dioxide by LPCVD (see, for example Wolf and Tauber, page 184, last full sentence); Havemann (US 5,565,384) further discloses that the organic-containing dielectric layer (54) can be applied by spinning (i.e. a coating method) (also see column 4, lines 7-11); and Havemann (US 5,565,384) further discloses that contact holes are formed through layers 50, 54 to expose the silicide (48) and the contact holes are subsequently filled with conducting material to electrically connect the silicide contacts (48) to the patterned metal conductors (18) (also see column 6, lines 20-27).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Havemann (US 5,565,384) as applied to claims 1-3 above, respectively, and further in view of Gracias et al. (US 2004/0023515 A1).

As shown above, Havemann (US 5,565,384) anticipates claims 1-3 of the applicant's invention. Havemann (US 5,565,384) further discloses that the gaps between the patterned conductors (18) are filled with organic-containing low dielectric constant layer (22), which are limitations set forth in claims 5-7 of the applicant's invention. However, Havemann (US 5,565,384) lacks the limitation of a surface modifying layer, formed by using silane coupler or metal coupler, formed on the second insulating film, which are also limitations set forth in claims 5-7 of the applicant's invention. Gracias et al. teach that the surface of an organo-silicate glass can be modified using a silane-coupling agent (see abstract).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the structure of Havemann (US 5,565,384) by

applying a silane-coupling agent, as taught by Gracias et al., to the surface of the organic-containing layer of Havemann (US 5,565,384). Gracias et al. recognize that the silane-coupling agent improves adhesion to adjacent layers (see abstract).

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Havemann (US 5,565,384) as applied to claim 9 above, and further in view of Wolf and Tauber.

As shown above, Havemann (US 5,565,384) anticipates claim 9 of the applicant's invention. Havemann (US 5,565,384) further discloses that an inorganic dielectric layer (56) is formed over the organic-containing layer (54), that the contact holes are also formed through this layer, that silicon dioxide is an exemplary inorganic dielectric material, and that the inorganic dielectric layer (56) is planarized (also see column 4, lines 11-14, column 5, lines 45-46, and the Table), which are limitations set forth in claim 10 of the applicant's invention. However, Havemann (US 5,565,384) does not expressly teach or suggest using a vapor deposition method to form the inorganic dielectric layer (56) (e.g. silicon dioxide), which is also a limitation set forth in claim 10 of the applicant's invention. Wolf and Tauber teach that chemically vapor deposited (CVD) silicon dioxide films are widely used in VLSI processing, including as insulators between metal layers in multilevel metal systems (see paragraph bridging pages 182-183).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Havemann (US 5,565,384) with those of Wolf and Tauber in order to form the silicon dioxide inorganic layer of

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Havemann (US 5,565,384) by a CVD method as taught by Wolf and Tauber. Wolf and Tauber recognize that CVD methods are known in the art as one way to deposit silicon dioxide films for use as insulators in multilevel metal systems (see paragraph bridging pages 182-183).

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Havemann (US 5,482,894), Ference et al., Ha et al., and Komada teach interconnect structures that feature contact openings formed through multi-layered interlayers to electrically connect to semiconductor elements. Wu et al. teach the treatment of silicon dioxide films with surface modification films.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SWS

*Stephen W. Smoot*  
Patent Examiner  
Art Unit 2813